

REMARKS

No new matter has been added. The Applicant again requests entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,

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APPENDIX B

**(VERSION OF SUBSTITUTE SPECIFICATION EXCLUDING CLAIMS
WITH MARKINGS TO SHOW CHANGES MADE)**

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APPLICATION FOR LETTERS PATENT

for

**METHOD OF BALL GRID ARRAY (BGA) ALIGNMENT, METHOD OF TESTING,
ALIGNMENT APPARATUS AND SEMICONDUCTOR DEVICE ASSEMBLY**

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TITLE OF THE INVENTION

METHOD OF BALL GRID ARRAY (BGA) ALIGNMENT, METHOD OF TESTING, ALIGNMENT APPARATUS AND SEMICONDUCTOR DEVICE ASSEMBLY

BACKGROUND OF THE INVENTION

[0001] Field of the Invention. The present invention relates generally to alignment of contacts on an electronic device with corresponding electronic contacts of a corresponding circuit on a carrier substrate. More specifically, the present invention relates to the alignment of the discrete conductive elements of a ball grid array (BGA) type semiconductor device with terminal pads of a printed circuit board or other [higher level]higher-level packaging. The inventive method and apparatus are particularly suitable for testing or [low volume]low-volume production.

[0002] State of the Art. Surface mount technology employed in semiconductor device packaging has assisted in increasing integrated circuit density on a single carrier substrate while maintaining or even increasing functionality. In an effort to further increase integrated circuit density while improving functionality, semiconductor die size continues to decrease. As semiconductor packages decrease in size, various difficulties arise in the manufacture of the packaged semiconductor die as well as its assembly with carrier substrates such as printed circuit boards.

[0003] For example, a ball grid array (BGA) is a design of semiconductor device which includes an array of discrete conductive elements in the form of conductive balls, or bumps, disposed on a surface of the semiconductor device to be mounted to a carrier substrate. The array of discrete conductive elements is aligned with a mating array of conductive terminal pads formed on the carrier substrate, such as a printed circuit board. After proper alignment, the discrete conductive elements are electrically connected to the terminal pads. If the conductive elements comprise solder balls, this step typically includes a reflow process. However, in testing situations where only a temporary connection is required, simple contact of the conductive balls with the terminal pads may be sufficient. Proper alignment is crucial to effecting electrical contact. If the BGA device is misaligned with respect to the carrier substrate and terminal pads,

one or more of the discrete conductive elements of the array may not make sufficient contact with the corresponding terminals pad(s). This, of course, may result in an inoperative circuit.

[0004] As BGA semiconductor devices are developed into smaller packages such as, for example, fine pitch BGAs, the size of the conductive balls is reduced. Likewise, the pitch, or the lateral spacing between adjacent conductive balls, also decreases. The reduction of ball size and pitch requires greater accuracy and tighter tolerances during manufacturing. Similarly, alignment of a BGA semiconductor device with the carrier substrate becomes increasingly difficult. Accurate alignment is conventionally accomplished with expensive, automated pick and place equipment which requires extensive programming.

[0005] Such automated pick and place equipment requires independent set up and programming depending on the type of semiconductor device being aligned and assembled. Various parameters are required for [programing]programming and operation, such as the size of the semiconductor device, location of the semiconductor device with respect to the carrier substrate and semiconductor device orientation with respect to the carrier substrate. Different alignment techniques may be employed depending on the type of semiconductor device as well. For example, alignment techniques may differ based on whether the device is a BGA, a thin small outline package (TSOP), a quad flat pack (QFP) or some other type of device. A TSOP, QFP and other similar semiconductor devices typically include conductive elements in the form of leads disposed around a portion or all of the periphery of the semiconductor device while a BGA semiconductor device, on the other hand, carries the discrete conductive elements on a major surface of a semiconductor die or interposer substrate. The ability to align a semiconductor device having visible leads, such as with a TSOP or QFP, may be accomplished using optical or sight techniques looking down on the device and carrier substrate from above. However, this ability is greatly diminished, if available at all, when aligning discrete conductive elements on a BGA semiconductor device with the corresponding, [terminal facing]terminal-facing pads of a carrier substrate, since it would be necessary to view the array of discrete conductive elements and the terminal pads, retain such alignment in computer memory and then calculate correct alignment.

[0006] Alignment concerns are increased when the assembly or testing process is to be [low volume]low-volume production. For example in rework, in various testing procedures, or in custom or small build projects, it is not always practical to expend the resources in programming and setting up automated equipment to assemble relatively few components. Thus, alignment may be performed partially or wholly as a manual operation. Manual alignment of such assemblies is difficult and time consuming at best, particularly when alignment is further complicated by an inability to utilize optical or sight alignment techniques.

[0007] Attempts to remedy such alignment difficulties have not proven to achieve complete success. For example, one solution to aligning a BGA semiconductor device with mating terminal pads of a carrier substrate has been to form mating cavities in a surface of the carrier substrate, wherein the terminal pads are formed in the mating cavities. Each individual cavity is configured to receive one of the discrete conductive elements of the BGA semiconductor device to effect self alignment of the semiconductor device. While such an approach attempts to remedy alignment difficulties where optical or sight processes are difficult if not impossible to employ, the described approach is problematic in that it relies on the accuracy of forming properly dimensioned and located discrete conductive elements on the BGA semiconductor device. Also, as with other techniques, it still fails to allow for visual or optical assistance in effecting or confirming alignment of discrete conductive elements of the semiconductor device with the carrier substrate.

[0008] In view of the shortcomings in the state of the art, it would be advantageous to provide a method of aligning BGA or other arrayed discrete conductive [element type]element-type semiconductor devices with corresponding carrier substrates or other [higher level]higher-level packaging for attachment. Such attachment may be either permanent or temporary.

[0009] It would also be advantageous to provide a method of alignment, as well as an apparatus for performing such alignment which may be employed either manually or in conjunction with automated pick and place equipment. In the case of utilizing the method or apparatus in conjunction with automated equipment, it should be capable of easy implementation, without incurring excessive set up time or operational expense.

BRIEF SUMMARY OF THE INVENTION

[0010] One aspect of the invention comprises a method for aligning a semiconductor device package with a carrier substrate such as a printed circuit board. The method includes forming at least two apertures through the semiconductor device. The apertures pass from a first major surface of the semiconductor device to a second[and], opposing major surface of semiconductor device. The carrier substrate is provided with at least two alignment features, each alignment feature respectively corresponding with one of the apertures of the semiconductor device. The semiconductor device is placed over the carrier substrate and each alignment feature is aligned with its corresponding aperture formed through the semiconductor device.

[0011] Another aspect of the invention includes a method of testing a semiconductor device having a plurality of discrete conductive elements projecting from a major surface thereof. A carrier substrate is provided having a plurality of terminal pads arranged in a pattern to mate with the plurality of discrete conductive elements. At least two apertures are formed in the semiconductor device, each aperture passing from a first major surface to a second, opposing major surface of the semiconductor device. The carrier substrate is provided with at least two alignment features, each alignment feature respectively corresponding to one of the at least two apertures in the semiconductor device. The semiconductor device is placed over the carrier substrate with each of the apertures in the semiconductor device being aligned with its corresponding alignment feature on the carrier substrate. Each discrete conductive element is placed in electrical contact with a corresponding terminal pad and electrical test signals are passed between the semiconductor device and carrier substrate via the terminal pads of the carrier substrate.

[0012] The alignment features may include corresponding apertures formed in the carrier substrate. In such a case, a pin may be placed through each aperture of the semiconductor device and into each aperture formed in the carrier substrate. Such pins may be [non-conductive]nonconductive and may also serve as a means of fastening the semiconductor device to the carrier substrate for either permanent or temporary assembly.

[0013] The semiconductor device may be held in place during testing by having the ends of the pins configured to form a mechanical locking mechanism such that insertion of the pins through the [aperture]apertures of the semiconductor [devise]device and carrier substrate both aligns the semiconductor device and retains the semiconductor device on the carrier substrate until testing is completed. After testing is completed, the pins may be cut or otherwise removed such that the semiconductor device may be removed from the carrier substrate for further testing, processing or packaging.

[0014] In accordance with another aspect of the invention, an alignment tool is provided. The alignment tool includes a holding mechanism such as, for example, a vacuum quill on an alignment head configured for placement against a surface of a semiconductor device. Alternatively, the alignment head may employ a plurality of fingers which [grasp]grasps the semiconductor device by its periphery. In addition to the holding mechanism, an alignment mechanism is incorporated into the alignment head. For example, in one embodiment, at least two locating pins, adjacent the holding mechanism, are affixed to the alignment head. The locating pins are sized and positioned to be inserted through at least two corresponding apertures formed in the semiconductor device and into at least two corresponding apertures in a carrier substrate. The alignment tool may be configured for manual use or for use with an automated pick-and-place device. The operator may use the alignment tool to align the semiconductor device with the carrier substrate by both sight and touch as the pins are inserted into the appropriate apertures.

[0015] In another embodiment, the alignment head may include an optical instrument, such as a [light emitting]light-emitting device located to provide light through at least two apertures of a semiconductor device. The optical instrument may then be used to detect alignment features such as optical fiducial marks formed of a reflective coating and placed on the surface of the carrier substrate. The [light emitting]light-emitting device passes light through the at least two apertures and, upon proper alignment of the semiconductor device with the carrier substrate, the light will be reflected from the optical fiducial marks. The reflected light is then detected and registered to indicate that the semiconductor device is properly placed over the carrier substrate for mounting.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0016] The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

[0017] Figure 1 is a plan view of the mounting surface of a printed circuit board for a multi-chip module (MCM) according to one embodiment of the present invention;

[0018] Figure 2 is a plan view of the mounting surface of a semiconductor device according to one embodiment of the present invention;

[0019] Figure 3 is a perspective view depicting an alignment technique according to one embodiment of the present invention;

[0020] [Figure]Figures 4A and 4B depict aligning pins according to another embodiment of the present invention;

[0021] [Figure]Figures 5A, 5B, and 5C are plan views of various semiconductor devices according to additional embodiments of the present invention; and

[0022] [Figure]Figures 6A and 6B show alignment tools utilized in conjunction with aligning a semiconductor device and a carrier substrate according to further embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0023] Referring to FIGS. 1 and 2, a carrier substrate is shown in the form of a printed circuit board 10 for a multi-chip module (MCM). The printed circuit board 10 has multiple landing sites 12, each matched to the footprint of a semiconductor device 14 to be mounted thereon. Each landing site 12 includes an array of conductive terminal pads 16 as well as a pair of alignment features 18. The terminal pads 16 are formed in association with conductive traces of the printed circuit board 10 and are arranged in a pattern to mate with a plurality of discrete conductive elements 20 located on and projecting from a major surface of the semiconductor device 14. The semiconductor device 14 depicted in FIG. 2 shows a [BGA type]BGA-type semiconductor device wherein the discrete conductive elements 20 comprise an array of conductive bumps formed of solder or another conductive material such as a conductive epoxy or conductor-filled epoxy and located on a major surface of the semiconductor device 14. A pair of

apertures 22 [are]is formed in the semiconductor device 14 and [are]is located such that [they]the pair of apertures 22 will correspond with the pair of alignment features 18 found on the printed circuit board 10 during assembly of the semiconductor device 14 with the printed circuit board 10 when the former is placed in proper alignment over the latter.

[0024] The apertures 22 comprise small channels or passages, for example, 30 mils in diameter, formed through the package of semiconductor device 14 at locations where they will not interfere with the internal circuitry of the semiconductor device 14. FIG. 2 shows the apertures 22 to be located on a diagonal at opposite corners of the semiconductor device 14. The location and size of the apertures 22 may, and likely will, vary depending on the specific semiconductor device 14 being mounted and the specific printed circuit board 10 to which the semiconductor device will be mounted. The apertures 22 may be formed during the fabrication of the semiconductor device 14 as an integral feature of the semiconductor device or packaging thereof. However, in using [mass produced]mass-produced semiconductor devices for small build projects, or in rework processes, it may be more desirable to [formed]form the apertures 22 after manufacture of the semiconductor device 14 using a simple technique such as drilling or burning. Such a process might be performed easily and accurately using conventional numerically controlled (NC) or computer numerically controlled (CNC) machinery, as is commonly understood by those of ordinary skill in the art.

[0025] It is noted that in viewing FIGS. 1 and 2, the alignment features 18 and the apertures 22 appear to be placed on opposite diagonals. However, it is noted that the views shown in FIGS. 1 and 2 represent the respective major surfaces 24 and 26 of the printed circuit board 10 and the semiconductor device 14 which will [by]be mutually facing when semiconductor device 14 is mounted to printed circuit board 10. Thus, as the semiconductor device 14 is rotated over such that the discrete conductive elements 20 may make contact with the terminal pads 16, the apertures 22 reverse their relative [location]locations and are positioned along the same diagonal as the alignment features 18 on printed circuit board 10.

[0026] Referring to FIG. 3, a perspective view shows the semiconductor device 14 being assembled to the printed circuit board 10 according to one embodiment of the present invention. The alignment features of the printed circuit board [30]10 of the presently disclosed

embodiment include a set of holes 18', or channels, similar to those formed in the semiconductor device 14. While these holes 18' formed in the printed circuit board 10 are of [similar]a size and shape similar to the apertures 22 formed in the semiconductor device 14, they will be referred to as holes 18' for purposes of differentiating them from the apertures 22. Also, it is noted that the apertures 22 are formed through the semiconductor device 14, passing from the [mounted]mounting surface 26 to the [non-mounted]non-mounting surface 28, creating open passages through the device. On the other hand, the holes 18' in the printed circuit board 10 may be blind holes, or may be through holes passing from the mounting surface 24 of printed circuit board [30]10 to the non-mounting surface 30 thereof.

[0027] To align the semiconductor device 14 with the printed circuit board 10 such that discrete conductive elements 20 of the semiconductor device 14 appropriately interface with corresponding terminal pads 16, locating pins 32 are placed in the holes 18' of the printed circuit board 10 and in the apertures 22 of the semiconductor device 14. The locating pins 32 are appropriately sized to fit in the holes 18' and apertures 22 and may be formed such that a press [fit]fit- type connection is formed upon insertion of the locating pins 32. Prior to assembly of the semiconductor device 14 to the printed circuit board 10, the locating pins 32 may be placed into either the holes 18' or the apertures 22. However, in such a method of assembly, it is preferable that the locating pins 32 be placed into holes 18' of the printed circuit board 10 such that the locating pins 32 may be sighted through the apertures 22 of the semiconductor device 14 during an alignment and assembly operation. Alternatively, the semiconductor device 14 may be placed on the printed circuit board 10 and roughly aligned by sighting through the apertures 22 to the holes 18'. Actual alignment of semiconductor device 14 to printed circuit board 10 would then be effected by subsequently placing the locating pins 32 through both apertures 22 and holes 18'.

[0028] After alignment has been effected and the locating pins 32 are in the holes 18' and the apertures 22, subsequent operations may take place depending on the purpose of assembling the semiconductor device 14 with the printed circuit board 10. For example, with the locating pins 32 in place and after proper alignment, the semiconductor device 14 may be tested by passing electrical signals between the semiconductor device 14 and the printed circuit board 10 via the terminal pads 16 and mating discrete conductive elements 20. Another example would be

to permanently attach the semiconductor device 14 to the printed circuit board 10 by permanently securing each discrete conductive element 20 to its corresponding terminal pad 16 by techniques well known in the art which depend on the composition of discrete conductive elements 20. It is also possible that the semiconductor device 14 be temporarily attached to the printed circuit board 10 by mechanical means which shall be discussed in greater detail below. Temporary assembly may be desirable in small custom projects as well as in situations where handling of the assembled module was to take place in between multiple tests of the semiconductor devices 14 mounted [thereof]thereto.

[0029] As noted above, the locating pins 32 should be manufactured to mate with the holes 18' and apertures 22. Thus, as the size or shape of the holes 18' and [channels 32] apertures 22 may change from one assembly to another, so should the size or shape of the locating pins 32. It is preferable that the locating pins 32 be manufactured from a [non-conductive]nonconductive, [anti-static]antistatic material such as an appropriate polymer material. The use of an [anti-static]antistatic material reduces the chance of static discharge damaging the semiconductor device 14 while use of a [non-conductive]nonconductive material helps to avoid any interference with the electrical signals passing through the semiconductor device 14 or printed circuit board 10.

[0030] Various embodiments of the locating pins 32 may be utilized if it is desired that semi-permanent assembly be effected. For example, locating pins 32 as depicted in Figure 3 may be made from a thermoplastic or thermosetting material to enable thermal bonding of the locating pins 32 to the printed circuit board 10 and/or to the semiconductor device 14. Alternatively, Figures 4A and 4B show locating pins 32' and 32" respectively, which are configured to enable mechanical locking of the semiconductor device 14 to the printed circuit board 10.

[0031] Figure 4A depicts a pin 32' having a locking head 34 at each end [of the pin 32']thereof. The locking head 34 includes a region which is slightly enlarged with respect to the shank 36 of the pin 32', resulting in a slight shoulder 38 proximate each end. The locking head 34 has a cut or a slit 40 in it allowing the locking head 34 to compress slightly as it is passed through the aperture 22 or hole 18'. After the pin 32' has been properly inserted, the locking heads 34 will expand and shoulders 38 will retain a predetermined amount of pressure upon the non-mounting

surfaces 28 and 30 of the semiconductor device 14 and printed circuit board 10, respectively, to maintain the components in alignment.

[0032] Alternatively, Figure 4B shows a pin 32" with circumferential grooves 42 formed proximate each end thereof. In conjunction with installing pin 32" into the apertures 22 and holes 18', a c-clip or other retaining clip (not shown) may be received by each groove 42 after the pin 32" has passed through a hole 18' at one end thereof and an aperture 22 at the other end thereof. The retaining clips would then supply the requisite holding force to maintain the integrity of the assembly of the semiconductor device 14 and printed circuit board 10. Other, similar locking retaining mechanisms may be employed to accomplish the same purpose. Of course, various combinations of the [above described]above-described attaching methods and mechanisms may be used. For example, one end of a pin 32 may be thermally bonded in the holes 18' of the printed circuit board 10 while the opposite end of the pin 32 may include a mechanical fastening device. Also, it is contemplated that the pin 32 may be integrally formed with the printed circuit board 10 as the corresponding alignment features 18.

[0033] Just as the locating pins 32 may be utilized according to various embodiments, various sizes, shapes and arrangements of the apertures 22 (and thus the corresponding alignment features 18) may be utilized. Figures 5A, 5B and 5C depict some examples of different embodiments which may be used. Figure 5A shows a semiconductor device 14' wherein notch-shaped channels 44 are formed at the periphery of the semiconductor device 14'. It is noted that the channels 44 are shown to have a [semi-circular]semicircular shape as shown in this view. Other shapes, such as a simple notched "V", may also be sufficient. The channels 44 still pass from the non-mounting side 28' to the mounting side (not shown) of semiconductor device 14'. Figure 5B shows a semiconductor device 14" where the channels 46 and 46' are arranged asymmetrically with respect to the geographical outline of the semiconductor device 14" to facilitate proper rotational alignment of components. Figure 5C depicts a semiconductor device 14''' having a channel of a first size 48 and a channel of a second size 48' to facilitate proper rotational alignment of components. Thus, the embodiments shown in Figures 5B and 5C not only facilitate proper alignment of the semiconductor device with the printed circuit board, but also ensure proper orientation of a semiconductor device with respect to the printed circuit board[

to be assured]. Of course, in utilizing any of the embodiments described above, the alignment features 18 of the printed circuit board 10 are formed to correspond to the size, shape or arrangement of the apertures or channels of the semiconductor device. It is also noted that variations and combinations of the [above]above- described embodiments are contemplated as being within the scope of the invention. As an example, channels of different sizes may be arranged asymmetrically, or along the periphery.

[0034] Referring now to Figures 6A and 6B, placement tools 60 and 60' are respectively shown for assisting alignment of a semiconductor device 14 with a printed circuit board 10 in accordance with the technique described above. Figure 6A shows a holding mechanism in the form of a suction device 62 selectively connected to a vacuum source (not shown), which may be cup-shaped as shown or configured as a vacuum quill, for grasping and holding the semiconductor device 14. Alternatively, the holding mechanism may comprise a plurality of fingers or similar elements for grasping the semiconductor device about its periphery. In addition to the suction device 62, a pair of alignment pins 64 [are]is located adjacent the suction device 62 and [correspond]corresponds in size, shape and position with the apertures 22 formed in the semiconductor device 14. Because, as disclosed above, the apertures 22 correspond with the holes 18' of the printed circuit board 10, the alignment pins 64 will also correspond with the holes 18'. Thus, as the pins 64 are placed through the holes 18' of the printed circuit board 10, after being received in apertures 22, alignment of the semiconductor device 14 and printed circuit board 10 is effected. Subsequent to proper alignment and attachment of the semiconductor device 14 with the printed circuit board 10, whether temporary or permanent, the suction device 62 may be released and the tool 60 removed, including the alignment pins 64. Alternatively, the tool 60 may be constructed such that the pins are releasable from [aligning] placement tool 60 and remain with the assembled semiconductor device 14 and printed circuit board 10 and are replaced with respect to the tool 60 each time a semiconductor device 14 is placed on a printed circuit board 10.

[0035] Figure 6B shows a method of using a placement tool 60' wherein the tool 60' does not utilize any alignment pins. Rather, the tool 60' allows access for sighting through the apertures 22 of the semiconductor device 14 to confirm alignment of the apertures 22 with

corresponding alignment features 18 provided on the printed circuit board 10. In regard to this embodiment, the alignment features 18 need not be holes as discussed above[,] but, instead, may be an alignment marking that is viewable through the apertures 22. For example, reflective markings may be placed at appropriate locations on the mounting surface [30]24 of the printed circuit board 10 such that reflection of light by the alignment features 18 may be recognized by an optical instrument 66 or by an operator. In this regard, a [light emitting]light-emitting diode (LED) mounted on an alignment tool may be used as a downwardly directed light source and the reflection thereof from markings comprising alignment features 18 detected by a photocell. When using an optical instrument 66 to recognize the reflection, thus effecting alignment, the optical instrument 66 may be integrated into the alignment tool 60' as depicted in Figure 6B.

[0036] While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for aligning a semiconductor device with a corresponding landing site on a carrier substrate. At least two apertures are formed in a semiconductor device, the apertures passing from a first major surface to a second, opposing major surface of the semiconductor device. Corresponding alignment features are provided on the carrier substrate at the landing site to which the semiconductor device is to be mounted. The alignment features are aligned with the corresponding apertures to effect alignment of the semiconductor device. The alignment features may include apertures corresponding in size, shape and arrangement to the semiconductor device apertures. [An alignment pin]Alignment pins may be placed through the at least two[sets of] apertures[and] to assist with alignment.

APPENDIX D

**(VERSION OF CLAIMS AS AMENDED HEREIN
WITH MARKINGS TO SHOW CHANGES MADE)**

(Serial No. 09/944,472)

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for aligning a semiconductor device with a carrier substrate for electrical interconnection therebetween, the method comprising:
forming at least two apertures through the semiconductor device from a first major surface thereof to a second[and], opposing major surface thereof;
providing a major surface of the carrier substrate with at least two alignment features spaced and positioned in respective correspondence to the at least two apertures;
placing the semiconductor device over the carrier substrate; and
aligning the at least two apertures formed in the semiconductor device with the at least two alignment features of the carrier substrate.
2. (Amended) The method of claim 1, wherein aligning the at least two apertures with the at least two alignment features includes sighting each alignment feature of the at least two alignment features through a respective corresponding aperture of the at least two apertures.
3. (Amended) The method of claim 1, wherein providing the major surface of the carrier substrate with at least two alignment features includes forming at least two holes in the carrier substrate.
12. (Amended) The method of claim 3, wherein placing the semiconductor device [on] over the carrier substrate is effected using a pick and place device.
14. (Amended) The method of claim 13, further including lifting the pick and place device including the[locating] pins from the aligned semiconductor device and carrier substrate.
15. (Amended) The method of claim 1, wherein providing the major surface of the carrier substrate with at least two alignment features [in the carrier substrate] includes forming at least two pins on the carrier substrate.

17. (Amended) The method of claim 1, wherein providing the major surface of the carrier substrate with at least two alignment features [in the carrier substrate] includes forming optically perceptible marks on the carrier substrate.

21. (Amended) The method of claim 20, wherein providing the major surface of the carrier substrate with at least two alignment features [on the carrier substrate] includes correlating a size of each of the at least two alignment features with a size of [each of] a respectively corresponding aperture of the at least two apertures.

24. (Amended) A method of testing a semiconductor device having a plurality of discrete conductive elements disposed in a pattern on a surface thereof, the method comprising:
providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements;
forming at least two apertures in the semiconductor device, each aperture passing from a first surface thereof to a second, opposing surface thereof;
providing the carrier substrate with at least two alignment features, each alignment feature respectively spaced and positioned in correspondence to one of the at least two apertures;
placing the semiconductor device over the carrier substrate;
aligning each aperture of the at least two apertures formed in the semiconductor device with a [respectively] corresponding alignment feature of the at least two alignment features of the carrier substrate;
electrically contacting each discrete conductive element of the plurality with a terminal pad of the plurality; and
passing at least one electrical signal between the semiconductor device and the carrier substrate.

25. (Amended) The method of claim 24, wherein aligning each of the at least two apertures with a corresponding alignment feature of the at least two alignment features includes sighting each alignment feature through a [respectively] corresponding aperture.

28. (Amended) The method of claim 26, wherein aligning each of the at least two apertures with a corresponding alignment feature of the at least two alignment features includes placing pins through the at least two apertures and into the at least two holes.

29. (Amended) The method of claim 28, further comprising forming the pins of a non-conductive material.

33. (Amended) The method of claim 29, further comprising forming a mechanical self-locking mechanism proximate at least one end [thereof]of each pin.

34. (Amended) The method of claim 29, further comprising removing the pins subsequent to the alignment of each of the at least two apertures with a corresponding alignment feature of the at least two alignment features.

35. (Amended) The method of claim 27, wherein placing the semiconductor device [on]over the carrier substrate includes[is effected] using a pick and place device.

37. (Amended) The method of claim 36, further including lifting the pick and place device including the [locating]pins from the[aligned] semiconductor device and carrier substrate.

39. (Amended) The method of claim 38, wherein forming pins on the carrier substrate includes forming a mechanical locking mechanism proximate an end of each of the pins.

40. (Amended) The method of claim 25, wherein providing at least two alignment features in the [printed circuit board]carrier substrate includes forming at least two optically perceptible marks on the carrier substrate.

42. (Amended) The method of claim 41, wherein sighting the at least two optically perceptible marks [one]on the carrier substrate through the at least two apertures is effected using an optical instrument.

43. (Amended) The method of claim 25, wherein the at least two apertures are each defined by a diameter and wherein the method further comprises forming at least one of the at least two apertures with a larger diameter than that of at least one other aperture of the at least two apertures.

44. (Amended) The method of claim 43, wherein providing at least two alignment features on the [printed circuit board]carrier substrate includes correlating a size of each alignment feature of the at least two alignment features with a size of a[respectively] corresponding aperture of the at least two apertures.

47. (Amended) An alignment tool for aligning a semiconductor device with a carrier substrate comprising:

a head including a holding mechanism including structure for releasably holding a semiconductor device;
an alignment structure carried at least in part by the head, associated with the holding mechanism and configured to effect alignment of at least two apertures formed through [a]the semiconductor device with at least two corresponding alignment features formed on a carrier substrate when the semiconductor device is superimposed over the carrier substrate.

48. (Amended) The alignment tool of claim 47, wherein the at least two corresponding alignment features comprise holes formed in the carrier substrate and wherein the alignment structure includes at least two pins carried by the head, the at least two pins being configured, spaced and positioned for insertion through the at least two apertures and into the at least two corresponding holes.

50. (Amended) The alignment tool of claim [47]48, wherein the head and the at least two pins are configured for removal of the at least two pins from the alignment tool after insertion of the at least two pins through the at least two apertures of the semiconductor device and the at least two corresponding holes of the carrier substrate.

54. (Amended) The alignment tool of claim [47]48, wherein the at least two pins are fixed to the alignment tool.

55. (Amended) The alignment tool of claim [47]48, wherein the at least two pins each have a diameter, and wherein one of the at least two pins has a larger diameter than at least one other pin of the at least two pins.

56. (Amended) The alignment tool of claim [47]48, wherein the at least two pins are arranged asymmetrically.

57. (Amended) The alignment tool of claim 47, wherein the at least two corresponding alignment features comprise optically perceptible markings and wherein the alignment structure is adapted to optically detect the optically perceptible markings.

58. (Amended) The alignment [head]tool of claim 57, wherein the alignment structure is located and adapted to detect the optically perceptible [marks]markings by sighting through the at least two apertures when the semiconductor device is held by the holding mechanism.